



UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/731,064

12/09/2003

Todd Arthur Cannon

ROC920030228US1

3760

7590

02/15/2006

Robert R. Williams
IBM Corporation - Dept. 917
3605 Highway 52 North
Rochester, MN 55901

EXAMINER

ROSSOSHEK, YELENA

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,064	CANNON ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,8-11 and 13-16 is/are rejected.
- 7) ☒ Claim(s) 5-7 and 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the Application 10/731,064 filed 12/09/2003.
2. Claims 1-16 are pending in the Application.

Oath/Declaration

3. Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Claim Objections

4. Claims 2-8, 10-13, 15 and 16 are objected to because of the following informalities: claims 2-8, 10-13, 15 and 16 have insufficient antecedent basis issue.

Claim 1 line 9 after "planes" delete ",", insert --;--

Claim 14 line 1 before "Apparatus" insert --An--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4, 8-11, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando et al. (US Patent 6,550,037) further in view of Tetelbaum (US Patent Application Publication 2005/00606675).

With respect to claims 1 and 9 Ando et al. teaches a method for implementing automated detection of excess aggressor shape capacitance coupling in printed circuit board (PCB) layouts within a method for designing a decoupling circuit for a source line of a LSI to be disposed on a printed circuit board (col. 2, ll.27-29), a computer program product for implementing automated detection in a computer system within computer aided design system for automated generating decoupling circuit design (col. 7, ll.31-34), comprising the steps of: receiving a PCB design file containing an electronic representation of a printed circuit board design as shown on the Fig. 6 receiving LSI library 10 storing a variety of object LSI to be mounted on the PCB (col. 3, ll.59-62) and PCB library 12 storing the information for a variety of PCBs (col. 4, ll.6-13); identifying a list of candidate shapes, the candidate shapes disposed on layers adjacent to power planes within LSI 51 shown on the Fig. 1 which is a candidate shapes adjacent to noise generating by power source 54 (power plane) (col. 3, ll.32-38); calculating a capacitance coupling the candidate shapes to adjacent noise-generating planes within the decoupling capacitor designing block 14 for determination the capacitance of the decoupling capacitor (col. 4, ll.27-32), and determining a ratio of each the calculated coupling capacitance and a decoupling capacitance connecting the respective candidate shape to a reference plane within determination of the decoupling capacitor 52 shown on the Fig. 1 prepared by the decoupling capacitor designing section 14 and an allowable multiplexing ratio (col. 4, ll.37-44). However Ando et al. lacks the specifics regarding a list of candidate shapes. Tetelbaum teaches identifying a list of candidate shapes within generating a list of only noise critical nets (candidate shapes) from the

representation of the resistance graph using a SPEF file for an integrated circuit design as input as shown on the Fig. 6 (paragraph [0009]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Tetelbaum to teach the specifics subject matter Ando et al. does not teach, because a computer program product for analyzing noise for an integrated circuit design is used (paragraph [0165]).

With respect to claim 14 Ando et al. teaches an apparatus for implementing automated detection of excess shape coupling in printed circuit board (PCB) layouts within computer aided design system for automated generating decoupling circuit design (col. 7, ll.31-34) comprising: an excess shape coupling detection program for receiving a PCB design file containing an electronic representation of a printed circuit board design as shown on the Fig. 6 receiving LSI library 10 storing a variety of object LSI to be mounted on the PCB (col. 3, ll.59-62) and PCB library 12 storing the information for a variety of PCBs (col. 4, ll.6-13; for using the PCB design file for identifying a list of candidate shapes, the candidate shapes disposed on layers adjacent to aggressor planes within LSI 51 shown on the Fig. 1 which is a candidate shapes adjacent to noise generating by power source 54 (power plane) (col. 3, ll.32-38); for calculating an effective capacitance coupling the candidate shapes to adjacent noise-generating planes within the decoupling capacitor designing block 14 for determination the capacitance of the decoupling capacitor (col. 4, ll.27-32); for determining a ratio of each the calculated effective capacitance and a decoupling capacitance connecting the respective candidate shape to a reference plane within determination of the decoupling

capacitor 52 shown on the Fig. 1 prepared by the decoupling capacitor designing section 14 and an allowable multiplexing ratio (col. 4, ll.37-44). However Ando et al. lacks the specifics regarding a list of candidate shapes, sorting determined ratios, a user interface. Tetelbaum teaches identifying a list of candidate shapes within generating a list of only noise critical nets (candidate shapes) from the representation of the resistance graph using a SPEF file for an integrated circuit design as input as shown on the Fig. 6 (paragraph [0009]); for sorting the determined ratios to produce a ranked list of the candidate shapes within filtering victim nets by comparison coupling ratio (paragraph [0091]), wherein coupling ratio is ratio between coupling capacitance to the total net capacitance (paragraph [0072]); and a user interface for displaying the ranked list of the candidate shapes for user review within a computer program product for analyzing noise for an integrated circuit design having attributes of computer system including monitor to display the steps of executing instruction for the integrated circuit design (col. paragraphs [0164] – [0174]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Tetelbaum to teach the specifics subject matter Ando et al. does not teach, because a computer program product for analyzing noise for an integrated circuit design is used (paragraph [0165]).

With respect to claims 2-4, 8, 10, 11, 13, 15 and 16 Tetelbaum teaches:

Claim 2: includes the step of sorting the determined ratios and providing a ranked list of shape names using the sorted ratios within filtering victim nets by comparison coupling ratio (paragraph [0091]), wherein coupling ratio is ratio between coupling capacitance to the total net capacitance (paragraph [0072]);

Claims 3, 10, 15: wherein the step of providing the ranked list of shape names includes providing the ranked list of shape names with the determined ratio, an area, and a location of the shapes within step 622 of the Fig. 6 by creating a report noise violation including victim's name (paragraphs [0118]), [0142]);

Claim 4: wherein the step of identifying the list of candidate shapes includes identifying the candidate shapes disposed on layers adjacent to power planes and having an assigned name that indicates usage for power distribution within the report noise violation, wherein noise analysis includes dependency the value of noise from voltage state (paragraph [0074]);

Claims 8, 13: wherein the determined ratio of each the calculated effective capacitance and the decoupling capacitance connecting the respective candidate shape to a reference plane is used to produce a ranked list of the candidate shapes for user review within filtering victim nets by comparison coupling ratio (paragraph [0091]), wherein coupling ratio is ratio between coupling capacitance to the total net capacitance (paragraph [0072]) using a computer program product for analyzing noise for an integrated circuit design having attributes of computer system including monitor to display the steps of executing instruction for the integrated circuit design (col. paragraphs [0164] – [0174]).

Claims 11, 16: wherein the step of identifying the list of candidate shapes includes identifying the candidate shapes having a predefined assigned name indicating usage (claim 8 on Page 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Tetelbaum to teach the specifics subject matter Ando et al. does not teach, because a computer program product for analyzing noise for an integrated circuit design is used (paragraph [0165]).

Allowable Subject Matter

7. Claims 5-7 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach the step of calculating the effective capacitance coupling the candidate shapes (victim) to adjacent noise-generating planes includes steps of identifying an overlap area of the candidate shapes to each adjacent noise-generating plane; representing a distance between the candidate shapes (victim) and the adjacent noise-generating (aggressor) planes and permittivity of the dielectric layers; the steps of calculating an interlayer parallel-plate effective capacitance represented by: $C_{pp} = \epsilon A / D$ where, A = Plane and candidate shape overlap area (Meter.sup.2) $\epsilon = \epsilon_r * \epsilon_0$, where ϵ_r represents relative permittivity ϵ_0 equals a predefined constant value Farads/Meter; (permittivity of free space) D = the distance (Meters) between the candidate shape and the adjacent plane.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

STACY A. WHITMORE
PRIMARY EXAMINER

A handwritten signature in black ink, appearing to be "Stacy A. Whitmore", written over the printed name.